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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,029	12/28/2001	Konstantin Volodarsky	042496 0269289	3769

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EXAMINER	
WILKINS III, HARRY D	
ART UNIT	**PAPER NUMBER**
1742	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/041,029	VOLODARSKY ET AL.	
	Examiner	Art Unit	
	Harry D Wilkins, III	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *68-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *68-90* is/are rejected.

7)☒ Claim(s) *71 and 89* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. All previous grounds of rejection have been withdrawn in view of Applicant's amendments to the claims requiring liquid to be used in the upper section. Kamikawa (EP 0855736) does not contemplate using liquids in the upper chamber.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 13 August 2004 has been entered.

Claim Objections

3. Claims 71 and 89 are objected to because of the following informalities: In lines 2-3, claim 71 recites "from a group consisting essentially of ...", which is improper Markush language. It is suggested that this claim be amended to read "selected from a group consisting of ...". In line 5, claim 89 recites "carrying out a second third processing step", "second" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 65-70 and 73-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admission of prior art in view of Kamikawa et al (US 6,050,275).

Applicant admits as prior art (see specification from page 1, line 15 to page 4, line 2) a two step processing scheme including polishing/etching of a semiconductor substrate to remove conductive material from the wafer (i.e.-ECMD) followed by carrying out a second processing step including rinsing/cleaning. Thus, Applicant's admission teaches the two-step process of first removing conductive material and then rinsing/cleaning.

Thus, Applicant's admission fails to teach carrying out the method by first lowering the wafer into a lower section of a chamber, raising the wafer from the lower section to an upper section and positioning a movable guard between the lower section and the upper section that is liquid tight.

Kamikawa et al teach (see abstract, figs. 4, 10 and 15 and schematically in figs. 16-27, and col. 10, line 55 to col. 11, line 8) a method of performing a two step process on a semiconductor wafer including lowering the wafer into the lower section of a

chamber, performing a first process, then raising the wafer to the upper section of the chamber, positioning a movable guard 72 between the upper and lower sections that provides a fluid tight seal thereby preventing flow of fluids from the upper section to the lower section and performing a second processing step on the wafer. The scheme of Kamikawa et al had the advantage of avoiding detrimental results, such as oxide growth during transfer of the wafer or splattering of the processing liquid from the lower section of the chamber during further processing.

Therefore, it would have been obvious to one of ordinary skill in the art to have applied the movement scheme taught by Kamikawa et al with the prior art ECMD method because the scheme of Kamikawa et al prevents exposure of the wafer to atmosphere thereby preventing oxidation and other defects or side effects from being formed by keeping the wafer isolated in one chamber for both the ECMD step and the cleaning/rinsing step.

Regarding claim 66, the ECMD method taught by Applicant's admission includes polishing and etching.

Regarding claim 67, the second step in the ECMD method taught by Applicant's admission includes rinsing/cleaning.

Regarding claims 73 and 74, the ECMD method taught by Applicant's admission includes electrochemically depositing the conductive material and electrochemically removing the conductive material.

Regarding claim 75, Applicant admits as prior art (see page 3, line 8-12) that secondary etching operations were carried out. Thus, it would have been obvious to

one of ordinary skill in the art to have applied the scheme of Kamikawa et al to these other processes because the scheme of Kamikawa et al allowed for continuous processing steps without exposure to the atmosphere/environment in between steps.

Regarding claim 87, it would have been within the expected skill of a routineer in the art to have disposed the wafer in any suitable orientation, either vertically or horizontally.

Regarding claims 68 and 89, as above, Applicant's admission includes a "second" step of ECMD and a "third" step of rinsing/cleaning. Thus, Applicant's admission fails to teach that there was a "first" step performed in the upper chamber.

However, since the wafer being placed into the chamber at the start might have the disclosed contaminants on it from exposure to the atmosphere/environment, one of ordinary skill in the art would have been motivated to have performed an additional cleaning/rinsing step in order to ensure the quality of the wafer surface.

Regarding claim 70, the first processing step would be a cleaning/rinsing step.

Regarding claim 88, it would have been within the expected skill of a routineer in the art to have disposed the wafer in any suitable orientation, either vertically or horizontally.

Regarding claims 76-78 and 69, the prior art ECMD process included electrochemically depositing the conductive material and electrochemically removing the conductive material from the wafer to polish/etch the wafer.

Regarding claim 90, the third processing step would be a cleaning/rinsing step.

Regarding claim 79, Applicant's admitted prior art in view of Kamikawa et al teach a method including removing conductive material from a wafer in a first chamber, transferring the wafer to a second chamber located vertically above the first, isolating the first and second chambers using a movable guard that was adapted to provide a fluid tight seal and cleaning/rinsing the wafer with a liquid whereby the movable guard prevents the liquid from entering the first chamber.

Regarding claim 80, the ECMD process also includes depositing the conductive material on the wafer.

Regarding claim 81, Applicant's admission of prior art teaches the claimed ECMD process.

Regarding claims 82 and 83, the ECMD process includes electrochemically polishing the conductive material on the wafer.

Regarding claim 84, the ECMD process was followed by a rinsing process.

Regarding claim 85, Applicant's admitted prior art suggests performing a further etching step on the wafer (see page 3, lines 8-12).

Regarding claim 86, it would have been within the expected skill of a routineer in the art to have disposed the wafer in any suitable orientation, either vertically or horizontally.

7. Claims 71 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admission of prior art in view of Kamikawa et al (US 6,050,275) as applied to claims 65-70 and 73-90 above, and further in view of Matsukawa et al (US 5,518,542).

The teachings of Applicant's admission in view of Kamikawa et al are discussed above.

However, Applicant's admission and Kamikawa et al do not teach a step of providing a gas to the surface of the workpiece including O_2, CF_4, Cl_2, NH_2, nor the further step of heating the wafer while the gas was provided.

Matsukawa et al teach (see Example 3) using CF_4 gas for etching of silicon wafer substrates.

Therefore, it would have been obvious to one of ordinary skill in the art to have added an additional step as taught by Matsukawa et al of exposing the wafer to a CF_4 gas in order to ensure proper etching of the wafer surface.

Regarding claim 72, Kamikawa et al teach (see fig. 4) including heating means in the upper section of the chamber. It would have been within the expected skill of a routineer in the art to have applied the heat during any processing step where the application of such heat was known to add beneficial results, such as improving the etching results of CF_4.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry D Wilkins, III whose telephone number is 571-272-1251. The examiner can normally be reached on M-Th 10am-8:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy V King can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Harry D Wilkins, III
Examiner
Art Unit 1742

hdw